K_a-BAND MONOLITHIC GaAs POWER FET AMPLIFIERS*

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ABSTRACT

GaAs power MMIC amplifiers with an optimized FET structure operating at K_a-band have achieved a small-signal gain of 4.3 dB and an output power of 481 mW. These 1.7 x 0.9-mm MMICs include DC-blocking capacitors and bias networks. A cascaded four-stage amplifier has achieved a power gain of 18.9 dB and output power of 437 mW at 28 GHz. These results may represent the highest power/gain yet demonstrated from cascaded stages of MMICs with on-chip bias and DC blocking at K_a-band.

INTRODUCTION

The technology of millimeter-wave systems for satellite communications, phased-array, and electronic warfare systems applications is advancing rapidly. Progress in GaAs technology has led to the development of millimeter-wave power FETs and monolithic circuits, and respectable RF performance has been achieved at about 30 GHz. Recently, Noguchi et al. [1] have reported an MMIC amplifier with 21.1 dBm of output power and 3.7 dB of linear gain at 28 GHz. An on-chip, internally matched pseudo MMIC FET providing 1.1 W of output power and 4 dB of linear gain was achieved by Kobiki et al. [2], using an external DC-blocking and bias network. Kim et al. [3] used short unit-gate-width devices to demonstrate over 17.5-percent power-added efficiency, but at a power level of 75 mW.

This paper describes results obtained with K_a-band MMICs based on an optimized device structure and a circuit design approach intended to provide the best tradeoff among output power, linear gain, and power-added efficiency. Repeatable DC and RF performance was obtained from samples of four different processing runs. A circuit design including DC-blocking and bias networks was emphasized, and cascadable and electrically stable multistage MMICs achieved usable power gain at K_a-band. The results presented here demonstrate the achievement of high output power/total gain for the largest number of cascaded stages at 28 GHz, using MMICs with built-in DC-blocking capacitors and bias networks.

DEVICE STRUCTURE

The basic FET structure is similar to that used in an MIC amplifier providing better than 1 W of output power and 30-percent power-added efficiency at 20 GHz [4]. However, for K_a-band applications the device unit gate width has been reduced from 75 to 50 μm. The total gate width becomes 1 mm instead of 1.5 mm per unit cell for the K-band device. This effectively reduces gate resistance and results in a more reasonable impedance level for circuit matching.

Figure 1 is a SEM photograph of a FET taken from an MMIC. The nominal gate length is 0.45 μm. The recessed gate is offset toward the source to reduce gate-source resistance. To enhance the power combining efficiency of the 20 gate fingers, the lateral dimension of the FET is kept small by using narrow (~8 μm) source and drain fingers. For the millimeter-wave FET, a small lateral dimension is essential in order to minimize the transverse voltage standing-wave effect, which will cause inefficient power combining of the gates as well as possible instability. The gates are combined by a gate bus bar, and the source pads are combined by air bridges across the gate bus bar. Through-substrate via-holes are located outside the FET source fingers in the source pad area. This arrangement eliminates the need for critical alignment of via-holes onto the source fingers during device fabrication, leading to high yield and a small FET lateral dimension.

AMPLIFIER DESIGN

An equivalent circuit model for the FET was first established by using an in-house device modeling computer program, COMFET, based on device physics, FET structure and material parameters, and the predicted performance from S-parameter measured results at frequencies up to 26 GHz. The optimal load was calculated from another in-house program, L-PULL, which uses the maximum breakdown voltage across the drain-to-gate terminals and the maximum drain current as criteria to arrive at the maximum linear output power and the corresponding optimal load presented to the device. The accuracy

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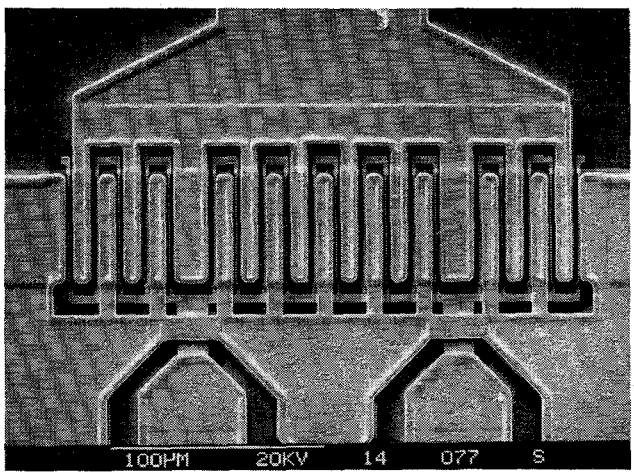

Figure 1. SEM Photograph of Power FET

of this load-pull program was previously verified in COMSAT's 30-GHz, MIC, 0.5-W power amplifier design.

The amplifier impedance matching circuit was designed to have a complex conjugate match at the input with an optimal load for maximum output power. In the MMIC implementation, the use of narrow high-impedance transmission lines was minimized to avoid excessive ohmic loss of the matching circuit. Instead, radial line open-shunted elements were used and shorted stubs were grounded through via-holes. Series and shunt capacitors were employed in the DC-blocking and bias networks, respectively. The amplifier circuit (especially the input) was optimized for input return loss and gain response by using computer-aided design programs such as SUPERCOMPACT and TOUCH-TONE. The chip size for the single-stage amplifier is 1.7 x 0.9 x 0.08 mm. Figure 2 is a photograph of the MMIC chip.

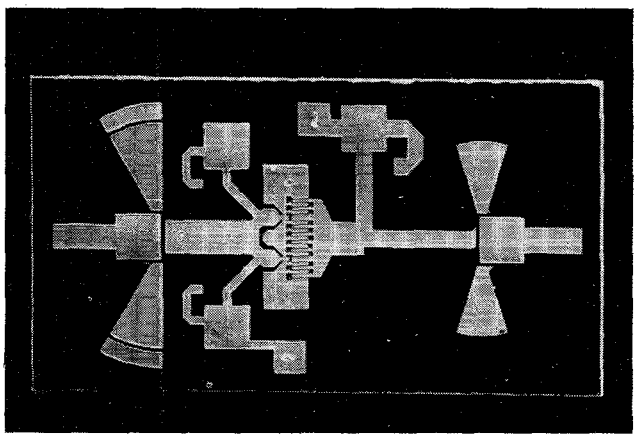

Figure 2. Photograph of K_a-Band Power MMIC

FABRICATION

The MMICs were fabricated using E-beam direct writing gate and photolithography. Vapor-phase epitaxy was employed to grow a buffer layer and an n and n^+ layer ($n - 2.5 \times 10^{17}$ cm^{-3}; $n^+ - 2 \times 10^{18}$ cm^{-3}) on the semi-insulating substrates. The chromium-doped substrates had been qualified to specifications and grown by the Bridgman method. Ohmic contacts consisting of an Au/Ge/Ni/Ag/Au alloy were fabricated by a lift-off technique. Metal-insulator-metal capacitor base metal was defined by lifting off Ti/Pt/Au. The dielectric layer was 5,000-Å-thick Si_3N_4, and the top plate metalization was Ti/Au at a thickness of 2 μm. Direct E-beam writing was used to define the gate length in PMMA resist for the recess gate channel etch and for the Ti/Pt/Au gate metalization. Plating-via/plating mask levels were employed to complete the air bridge structures. Figure 3 shows details of the gate structure and air bridges. Through-substrate via-holes were defined by IR and spray etching techniques to provide low-inductance grounding for the FET sources and the shunt capacitors.

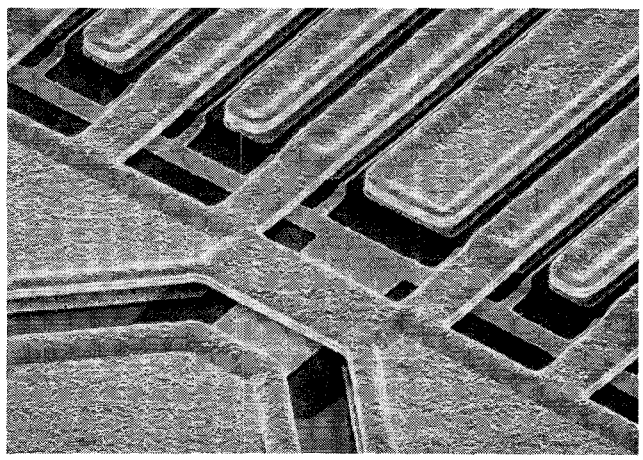

Figure 3. SEM Photograph of Gate and Air Bridges of the Power FET

MEASURED PERFORMANCE

To evaluate the MMICs accurately, a high-performance waveguide-to-microstrip transition was developed for the K_a-band. A ridged-waveguide approach was selected for its low RF loss advantage and rigid structure, which are compatible with space applications. Typical total RF loss, which includes two waveguide-to-microstrip transitions and two 2.54-mm fused silica 50-Ω transmission lines, is 0.3 dB. The measured performance is shown in Figure 4, and the return loss per waveguide-to-microstrip transition is better than 24 dB.

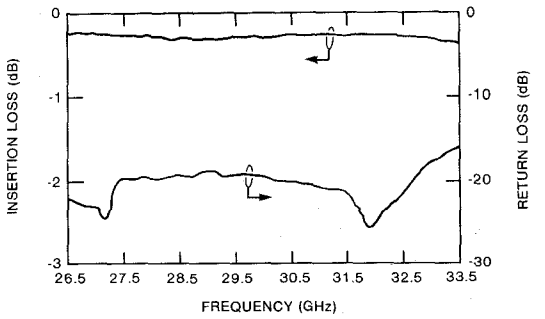

Figure 4. Measured Performance of Two Waveguide-to-Microstrip Transitions Plus Two 2.54-mm-Long 50-Ω Lines

All circuits from four wafer runs were on-wafer DC tested. Samples of MMICs were then individually RF tested to evaluate the consistency of their performance. Each diced amplifier module was mounted on a copper test fixture with bias feedthroughs, as well as 2.3-mm-long 50-Ω transmission lines at the input and output. The RF loss of these transmission lines was not deducted from the test results. This evaluation approach allows modules to be cascadable in a multistage amplifier configuration. Figure 5 is an example of the multistage amplifier assembly, showing four single-stage modules and two waveguide-to-microstrip transitions.

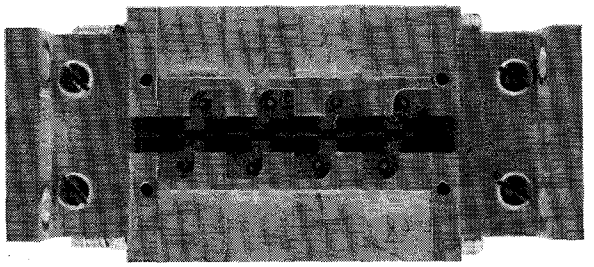

Figure 5. Assembly of the Four-Stage MMIC Amplifier With Waveguide-to-Microstrip Transitions

A single-stage MMIC amplifier at 28 GHz provided output power of 481 mW and linear gain of 4.3 dB at a power-added efficiency of 11.2 percent. Figure 6 shows the power transfer characteristics of this amplifier. The corresponding gain and input return loss vs frequency plots are shown in Figure 7, where the bandwidth with power gain exceeding 3 dB is 1.4 GHz (from 27.2 to 28.6 GHz). The higher frequency response of the MMIC obtained at a DC bias optimized for gain is also indicated. Typical drain and gate biases for power operation were 6 and -1.2 V, respectively, with a device breakdown voltage of 13 V. Some of these amplifiers are capable of producing 5 to 6 dB of gain at the maximum gain biases, and a maximum output power of 492 mW (0.49 W/mm). At a lower power level of 454 mW, a power-added efficiency of 14.3 percent was achieved.

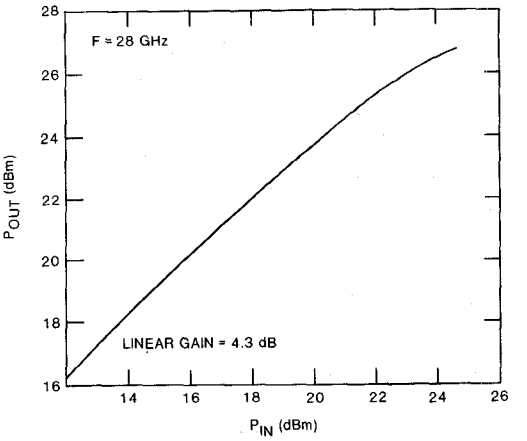

Figure 6. One-Stage K_a-Band Power MMIC Amplifier Performance

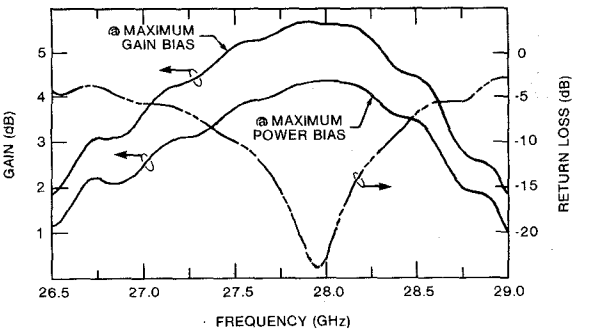

Figure 7. Gain and Input Return Loss vs Frequency of MMIC

A cascaded four-stage amplifier provided a linear gain of 18.9 dB and an output power of 437 mW at 28 GHz. The output power vs input power characteristic of this amplifier is shown in Figure 8. Stable power amplification was obtained in the direct cascading of the single-stage MMIC modules.

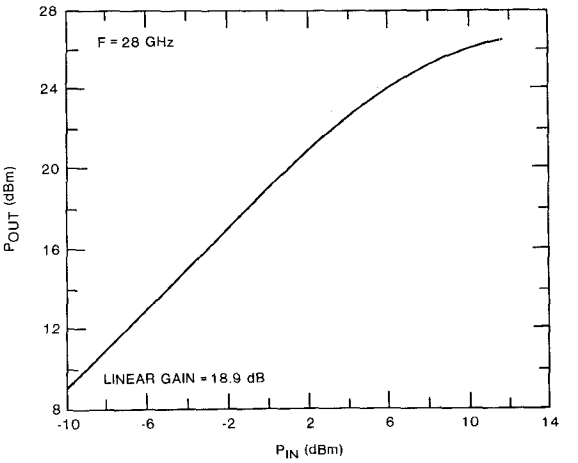

Figure 8. Four-Stage K_a-Band MMIC Amplifier Performance

CONCLUSIONS

Sub-half-micron-gate FET power MMICs have been shown to provide close to 0.5 W of output power at 28 GHz. High stable power gain was achieved through a cascadable multistage configuration. Further reduction in gate length and improvement in output power through parallel combining of the MMICs are currently being implemented.

ACKNOWLEDGMENTS

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